We claim:

1. In an integrated circuit chip including a plurality of metal layers, first and second supply potentials and at least two adjacent logic blocks, a modifiable circuit for coupling the at least two adjacent logic blocks, comprising:

a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks;

a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is located at said boundary of the at least two adjacent logic blocks; and

an interconnect formed between the at least two adjacent logic blocks by at least one of said first and second metal interconnect structures, wherein a state of said interconnect is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers.

2. The circuit of claim 1, wherein said first metal interconnect structure is coupled to one of said first and second supply potentials and said second metal interconnect structure is coupled to the other one of said first and second supply potentials.

3. The circuit of claim 2, wherein prior to programming, said first and second metal interconnect structures are coupled at a top metal layer.

4. The circuit of claim 2, further comprising multiples of said first and second metal interconnect structures coupled together to form a plurality of modifiable cycles, wherein each half cycle is modifiable at least once.

5. The circuit of claim 4, wherein one cycle is laid out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

6. The circuit of claim 5, wherein said ladder structure is arranged to form a cube-shaped structure.

7. The circuit of claim 6, wherein the first and second supply potentials comprise two buses located in a central region of said cube-shaped structure and are accessible at each of the metal layers.

8. The circuit of claim 5, wherein said ladder structure is arranged to form a spiral-shaped structure.

9. The circuit of claim 8, wherein the first and second supply potentials comprise buses accessible at each of the metal layers.

10. The circuit of claim 1, wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers.

11. The circuit of claim 1, wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of a plurality of via layers.

12. The circuit of claim 1, wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

13. The circuit of claim 1, wherein said first and second metal interconnect structures are not electrically coupled to each other at a top metal layer

thereby forming two interconnects between the at least two adjacent logic blocks.

14. The memory cell as in one of claims 10-13, wherein one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

15. The circuit of claim 13, wherein said first and second metal interconnect structures are arranged to form a ladder structure.

16. The circuit of claim 13, wherein said first and second metal interconnect structures are arranged to form an offset ladder structure.

17. The circuit of claim 13, wherein said first and second metal interconnect structures are arranged to form a stacked structure.

18. The circuit of claim 17, wherein said stacked structure comprises first and second alternating metal interconnect patterns.

19. The circuit of claim 18, wherein:

said first alternating metal interconnect pattern comprises first and second interspersed metal traces, and

said second alternating metal interconnect pattern comprises third and fourth interspersed metal traces, and

wherein said third and fourth interspersed metal traces form a mirror image of first and second interspersed metal traces.

20. The circuit of claim 19, wherein said first plurality of vias interconnect ones of said first and third interspersed metal traces and said second

plurality of vias interconnect ones of said second and fourth interspersed metal traces.

21. The circuit of claim 19, wherein the memory cell is programmed at any metal layer by forming an open circuit in each of said first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions, and coupling together a first portion of said first interspersed metal trace to a first portion of said second interspersed metal trace and coupling together a second portion of said first interspersed metal trace to a second portion of said second interspersed metal trace.

22. The circuit of claim 21, wherein said open circuits and coupling is not performed in regions where vias are located.

23. The circuit of claim 22, wherein said programming is reversible during a subsequent chip revision.

24. The circuit of claim 20, wherein the memory cell is programmed at any of a plurality of via layers by removing two vias and inserting two vias.

25. The circuit of claim 24, wherein said programming is reversible during a subsequent chip revision.

26. The memory cell as in one of claims 22-24, wherein one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.